Experimental Reliability Improvement of Power Devices Operated Under Fast Thermal Cycling

Dan Simon, Cristian Boianceanu, Gilbert De Mey, and Vasile Ţopa

***Abstract*— In automotive applications, the lifetime of the power transistors is limited by the number of power pulses, induced by, e.g., short-circuit or inductive clamping events. This letter presents a solution for reliability improvement of double-diffused metal–oxide–semiconductor transistors which operate under thermomechanical stresses generated during power cycling.**

***Index Terms*— Reliability, DMOS metallization, fast thermal cycling, repetitive pulse SOA, stress migration.**

I. Introduction

DUE to the high power densities dissipated in modern power devices, the transistor's area is not only given by the on-resistance, but it is also given by the number of power pulses the device can handle until failure [1]. In particular, DMOS transistors, which are used as switching elements in automotive applications, can fail after a limited number of switching cycles due to excessive thermo-mechanical stresses accumulated over their lifetime. Mechanical stresses are induced by high, non-uniform junction temperature variations generated during high power events e.g. switching-on of capacitive loads or switching-off of inductive loads. The repetitive power dissipation during the switching cycles (known as power cycling or fast thermal cycling) is below the temperature limit associated with the single-pulse-destruction SOA (safe-operating-area) boundary. Hence, power cycling determines a new set of SOA boundaries which are given by the maximum repetitive power pulses dissipated by a device [1].

One of the transistor failure modes, during fast thermal cycling, is triggered by electrical short-circuits between metal lines, as result of inter-metal dielectric (IMD) cracking [1]–[3]. This is caused by mechanical stresses which accumulate in the metallization (viscoplastic deformation) due to the mismatch of thermal expansion coefficients of the constitutive materials. This work focuses on reliability investigation of this failure mechanism and proposes an improvement method applied to DMOS (double-diffused metal oxide semiconductor) devices from a BCD (Bipolar-CMOS-DMOS) technology (typically used in multi-channel switch products). The problem is usually solved by careful design of the DMOS metallization structure, (e.g. optimizing the distances between metal lines [4]) and by other materials and technology related solutions [5], [6]. The disadvantage of the latter is that, sometimes, production costs are traded for better robustness.

The method proposed in this letter has the advantage that it further improves any design which was optimized from the layout or technology point of view. By conveniently controlling the power distribution in the device, the temperature distribution and, therefore, the mechanical stress distribution can be adjusted (stresses can be reduced or uniformly spread) and a higher lifetime is achieved. Another advantage of the method is that it does not degrade the on-state resistance of the device. Furthermore, the method can be applied to any technology (materials, number of metal layers etc.) susceptible to the studied failure mode.

II. Improvement Method

The key to DMOS lifetime improvement is mechanical stress adjustment in the power device's metallization system. This can be achieved by controlling the temperature distribution in the system, which can, in turn, be achieved by controlling the power distribution in the device. To be able to control the power distribution, the DMOS device is divided in several regions containing multiple DMOS cells. All regions share the same source and drain and each region has its own gate. Therefore, the power distribution can be adjusted by switching on/off gates which control different regions of the DMOS active area. In the target application, the total dissipated power is not changed and it is given by the load (e.g. on-state current through inductor). The advantage is that some of the transistor regions are switched-off temporarily, only during the high power event, so the on-resistance is not lost.

To verify the method, a test structure was manufactured in a BCD technology, with several thin metal layers and a thick power metal on top. The active area of the transistor is 0.15 mm^2 and it has an aspect ratio of 5:1, as shown in Fig.1, and the DMOS is built as described in the above paragraph.

From power cycling experiments, we found that DMOS devices from this technology fail after oxide cracking, followed by short-circuit between adjacent metal lines from the last thin metal layer, immediately beneath the power metal (Fig.1). This observation reduces our 3-D problem to a 2-D problem, because the destruction point (oxide crack) is pinned to a single plane.

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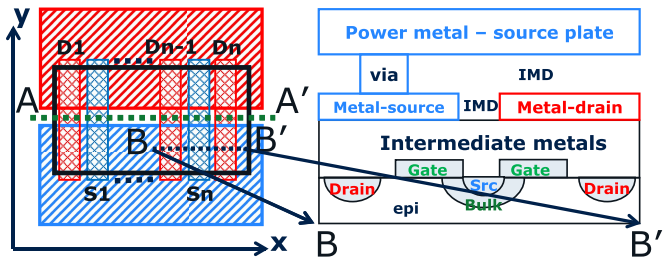

Fig. 1. Schematic representation of the DMOS structure with: full active area (black rectangle), power metal source and drain plates (blue and red).

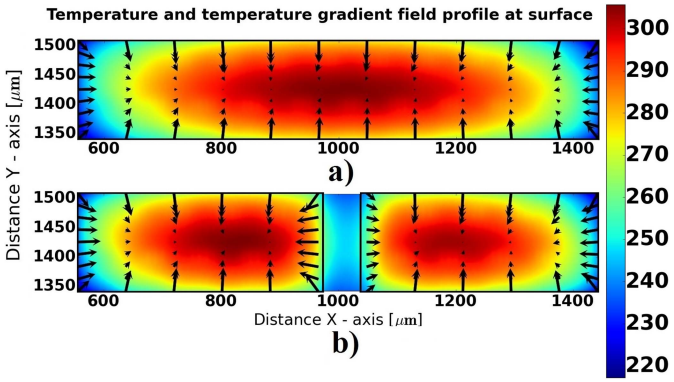

Fig. 2. Simulated temperature plot at the surface of the device, temperature gradients are indicated by arrows. Black borders delimit active area. a) Setup#1 - Full active area – all DMOS cells switched on. b) Setup#2 - Reduced active area - center DMOS cells switched off.

From [3] we expect that metal deformation and mechanical stress accumulation in metallization is proportional with and driven by temperature gradients. Metal migration starts in the regions of maximum temperature gradients and accumulates and generates peak mechanical stress in the regions of maximum temperature [3]. This applies to our case as shown in Fig.2.a, which depicts a typical 2-D temperature distribution simulated with the electro-thermal simulator presented in [7]. It can be observed that the highest temperature gradients (represented by black arrows) are at the edges of the device, and are pointing towards the center of the device. The maximum temperature of Fig.2.a (i.e. the hotspot) is in the center of the device. The metal lines from the last thin metal layer, of our device, are parallel to the Y – axis, as shown Fig.1. Therefore, the temperature gradients along Y-axis are the most important, because the metal can migrate easier along Y-axis than along X-axis (where IMD acts as a barrier).

Fig.2.a shows a temperature plot at the Silicon surface, for the typical case when all DMOS cells are switched-on. It can be seen that the hotspot is in the center of the device. If some of the center vertical stripes of DMOS cells are deactivated, a split structure results, with the total active area less than the original active area. Fig.2.b shows the temperature distribution at the surface of the Silicon for this last case, where the power dissipation is the same as in the first case. It can be seen that two hotspots appear in this case, symmetric to the vertical centerline. In Fig.2 the hotspots are on the same position with respect to the Y-axis. Therefore, deactivating vertical stripes of DMOS cells will move the hotspot and the peak mechanical stress on the same axis (AA' line in Fig.1), which further reduces our problem to one dimension.

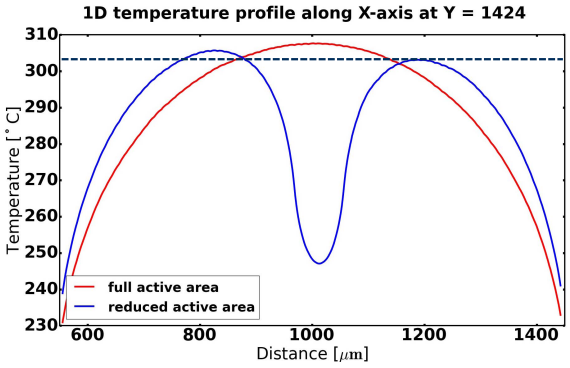

Fig. 3. Simulated temperature profile. Cut along AA' line of Fig.1 for temperature profiles of Fig.2.a (solid red line) and Fig.2.b (solid blue line).

III. Measurement Results

A. Thermo-Mechanical Stress Conditions

For the fast thermal cycling stress tests, the DMOS transistors were driven with periodic rectangular power pulses, at constant current. Due to flexibility reasons, the power pulses are emulated, via an external circuit (the tested devices do not operate with loads). In these tests the ambient junction temperature was 125°C and the peak junction temperature was 310°C.

DMOS transistors were thermo-mechanically stressed under the following two test conditions:

Setup#1: a test condition corresponding to the temperature distribution case of Fig.2.a (at the end of the power pulse), where all DMOS cells are switched-on (reference condition).

Setup#2: a test condition corresponding to the temperature distribution case of Fig.2.b, where center vertical stripes of DMOS cells are switched-off, resulting in a reduced active area (improved condition).

The number of DMOS cells to be deactivated was chosen such that the peak temperature reached in setup#2 is the same as the peak temperature reached setup#1. In spite of the very different temperature distributions, the peak temperatures are the same, as shown Fig.3 (temperature profile along the AA' cutline from Fig.1). While this situation may appear counterintuitive due to the higher power density, in the case of setup#2, a higher thermal capacitance is actually available, due to the Silicon volume of the disabled active area from the center of the device, where no power dissipation occurs [8]. It is important that the ambient temperature and the peak temperatures to be the same in both cases, because [1]–[3] state that the lifetime of power devices is directly proportional to these quantities.

In the case of the temperature profile of setup#2, the two hotspots which appear symmetrical to the center of the device (Fig.2.b and blue line of Fig.3) do not have exactly the same temperature. The hottest region is on the left hand side due to the small asymmetry introduced in the gate deactivation, i.e. the active area on the left side is a little bit larger than the active area on the right side. Therefore, the destruction point is pinned to the higher temperature region: the left hand side.

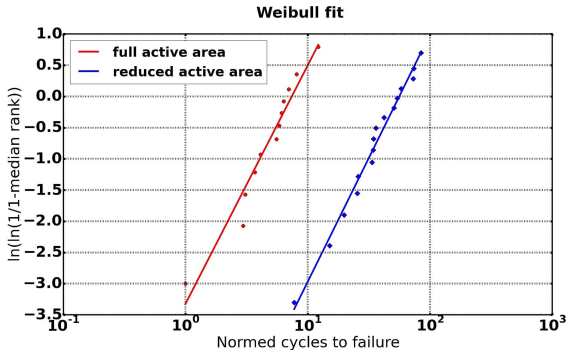

Fig. 4. Weibull fit of the lifetime data for DMOS devices operating under setup#1 conditions and setup#2 conditions.

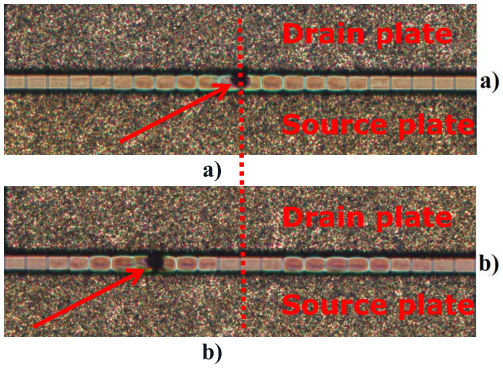

Fig. 5. Optical microscope images revealing destruction points for: a) setup#1; b) setup#2. Arrows indicate destruction point and dotted line indicates device center. The vertical dark lines are the IMDs between the thin metal lines.

B. Experimental Results & Discussion

The lifetimes of the DMOS devices, expressed in numbers of cycles to failure (normed to the earliest failure), are presented on a Weibull plot (Fig.4) for both setups. A significant higher characteristic life, by a factor of 7, is achieved for DMOS transistors which are operated under setup#2 conditions. Therefore, although the peak temperatures are the same in both cases, the temperature gradients also affect the lifetime of the power devices.

Optical microscope analysis (Fig.5.a) for all samples from the setup#1 test lot reveals that the destruction occurs in the center of the device, between adjacent stripes of the metal layer beneath the power metal (a portion of which can be seen between the two power metal plates). For the setup#2 test lot, the destruction point (Fig.5.b) appears again near the hotspot (Fig.2.b), which is away from the center of the transistor. The stressed regions can clearly be seen in Fig.5, i.e. the vertical thin metal lines are strongly deformed. Note that metal lines from the center of the device are not stressed and this is in accordance with the temperature profile of Fig.2.b, which corresponds to the deactivation of a fraction of the active area from the center of the device (setup#2).

Fig.6 shows a crack in the IMD which confirms that the destruction mechanism is the expected one. Fig.6 also shows deformation (i.e. voiding and thickness variations) of the metal lines. The crack formation was detected on a failed device,

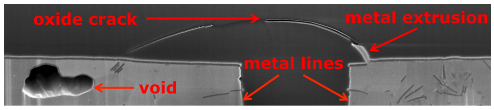

Fig. 6. FIB image of stressed device with IMD crack.

from setup#2 in a position symmetric to the burn-mark (the second hotspot from Fig.2.b).

IV. Conclusions

This letter has shown experimental results of an improvement method for the lifetime of power DMOS devices which operate under thermo-mechanical stresses induced by fast thermal cycling. Two test conditions were considered: setup#1 conditions, which generated a typical temperature distribution and setup#2 conditions, which generated a particular temperature distribution. In both cases the peak temperatures were the same but the temperature gradients were different. For setup#2, the power density was controlled (current redistributed), by switching off gates of DMOS cells, to obtain a particular temperature profile. The modified temperature conditions (temperature gradients) changed the thermo-mechanical stresses. Devices which operated under setup#2 conditions had a significant higher lifetime than devices which operated under setup#1 conditions.

The main advantage of the method is that it further improves a given layout or metallization scheme because the solution is to reduce or evenly spread the mechanical stresses by modifying the power distribution. Another advantage of the method is that only a simple, small circuit is needed to implement a gate control algorithm in an end-application. Finally, it should be mentioned that the on-state resistance of the device is not affected because DMOS cells are deactivated only during the power event.

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